R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, FIGS. 1, 3-6, 8 and 10-12 and in the specification as originally filed, for example, on page 7, lines 3-11, on page 9, line 17 through page 13, 19, on page 13, line 20 through page 15, line 17, on page 46, lines 1-17, and on page 48, line 3 through page 49, line 21. As such, no new matter has been introduced.

IN THE SPECIFICATION

The specification has been amended to update references to provisional and co-pending applications and to change the heading of the claims portion of the specification. No new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 12 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 6, 13, and 15-17 under 35 U.S.C. §102(b) as being anticipated by Chen (U.S. Patent no. 5,850,422) is respectfully traversed and should be withdrawn.

The rejection of claims 1, 2, 4, 5 and 15-17 under 35 U.S.C. §102(e) as being anticipated by Lee et al. (U.S. Patent No. 6,266,799; hereafter Lee) is respectfully traversed and should be withdrawn.

Chen is directed to an apparatus and method for recovering a clock signal which is embedded in an incoming data stream (Title of Chen). Lee is directed to multi-phase data/clock recovery circuitry and methods for implementing the same (Title of Lee). In contrast to Chen and Lee, the presently claimed invention (claim 1) provides **an analog circuit** configured to generate a plurality of samples of an input signal in response to a plurality of phases of a reference clock. Claims 15 and 16 recite similar limitations. Neither Chen nor Lee disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Specifically, assuming, *arguendo*, the data sampler 14 in FIG. 1 of Chen is similar to the presently claimed analog circuit (as suggested on page 3, lines 5-9 in section 6 of the Office

Action and for which Applicant's representative does not necessarily agree), Chen fails to disclose or suggest **an analog circuit** configured to generate a plurality of samples of an input signal in response to a plurality of phases of a reference clock, as presently claimed. In particular, FIG. 3 of Chen shows a more detailed diagram of the data sampler 14 in FIG. 1 of Chen. The data sampler 14 includes a number of D-type flip-flops and logic gates (column 4, lines 46-58 of Chen). A person of ordinary skill in the art would recognize a circuit including flip-flops and logic gates as being a digital circuit rather than an analog circuit as presently claimed. Therefore, the Office Action fails to meet the Office's burden to factually establish a *prima facie* case of anticipation by presenting a single prior art reference disclosing or suggesting each and every element of the presently claimed invention, arranged as in the present claims (M.P.E.P. §2132). As such, the presently claimed invention is fully patentable over Chen and the rejection should be withdrawn.

Furthermore, Chen teaches using a data signal as a strobe to sample a number of clock phases with the D-type flip-flops 40. A person of ordinary skill in the art would not consider a digital circuit comprising the number of flip-flops that uses a data signal as a strobe to sample a number of clock phases, as shown in Chen, to be the same as **an analog circuit** configured to generate **a plurality of samples of an input signal** in response to a plurality

of phases of a reference clock, as presently claimed. Therefore, the Office Action fails to meet the Office's burden to factually establish a *prima facie* case of anticipation by presenting a single prior art reference disclosing or suggesting each and every element of the presently claimed invention, arranged as in the present claims (M.P.E.P. §2132). As such, the presently claimed invention is fully patentable over Chen and the rejection should be withdrawn.

With respect to the rejection of claims 1, 2, 4, 5 and 15-17 under 35 U.S.C. §102(e) as being anticipated by Lee, the Office Action fails to meet the Office's burden to factually establish a *prima facie* case of anticipation by presenting a single prior art reference disclosing or suggesting each and every element of the presently claimed invention arranged as in the present claims. Specifically, assuming, *arguendo*, the four phase sampler circuit 302 in FIG. 3 of Lee is similar to the presently claimed analog circuit (as suggested on page 4, lines 9-12 of the Office Action and for which Applicant's representative does not necessarily agree), Lee does not appear to disclose or suggest **an analog circuit** configured to generate a plurality of samples of an input signal in response to a plurality of phases of a reference clock, as presently claimed. In particular, the four phase sampler circuit 302 in FIG. 3 of Lee includes a number of D-type flip-flops (see FIG. 4A and column 6, lines 44-55 of Lee). One skilled in the

art would consider a circuit implemented with D-type flip-flops to be a digital circuit rather than an analog circuit, as presently claimed. As such, Lee does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, assuming, *arguendo*, the data buffer 400 in FIG. 4A of Lee is similar to the presently claimed analog circuit (which was not suggested in the Office Action, but which Applicant's representative addresses for completeness), Lee does not appear to disclose or suggest an analog circuit configured to generate **a plurality of samples** of an input signal in response to a plurality of phases of a reference clock, as presently claimed. In particular, the data buffer 400 in FIG. 4A of Lee has a single output and, therefore, does not appear to generate a plurality of samples of the data signal (see FIG. 4A of Lee). Furthermore, Lee describes the output of the data buffer 400 as "a serial input (NRZ) data" (column 6, and column 6, lines 47-50 of Lee). One skilled in the art would not a data buffer converting a differential data signal to a single-ended data signal to be the same as generating a plurality of **samples** of the data signal, as presently claimed. As such, Lee does not disclose or suggest each and every element of the presently claimed invention, arranged as

in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 7-12, 14 and 18-20 under 35 U.S.C. §103 as being unpatentable over Lee in view of Williams et al. (U.S. Patent No. 6,417,698, hereafter Williams) is respectfully traversed and should be withdrawn.

Claims 7-12, 14 and 18-20 depend, directly or indirectly, from either claim 1 or claim 16, which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

New claims 21-23 depend, directly or indirectly, from either claim 1 or claim 16 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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